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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,326	07/03/2003	Daniel M. Kinzer	0400204D	4283

25700 7590 08/25/2010

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
08/25/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/613,326	KINZER ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-32,35,36,38,41-43 and 46-54* is/are pending in the application.

4a) Of the above claim(s) *48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-32,35,36,38,41-43,46,47 and 49-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/10/10,4/20/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of the embodiment of figures 1-8 in the reply filed on 07/23/2010 is acknowledged.

Claim 48 is withdrawn from consideration as being directed to non-elected embodiment.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 30-32, 35-36, 38, 41-43, 46-47 and 49-54 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the drawings and there is no adequate description in the disclosure for the claimed limitations of "a conductive path from said first power electrode to said second power electrode includes at least one vertical component oriented substantially perpendicular to said first major surface", as recited in claim 30.

There is no support in the drawings and there is no adequate description in the disclosure for the claimed limitations of "a conductive path from said source electrode to said drain electrode includes at least one vertical component oriented substantially perpendicular to said first major surface", as recited in claim 41.

There is no support in the drawings and there is no adequate description in the disclosure for the claimed limitations of "a conductive path from said first power electrode to said second power electrode includes at least one vertical component in said semiconductor die", as recited in claim 50.

There is no support in the embodiment of figures 1-8 for the claimed limitations of "a conductive path from said first power electrode to said second power electrode includes at least one vertical component oriented substantially perpendicular to said first major surface", and "a conductive path from said source electrode to said drain electrode includes at least one vertical component oriented substantially perpendicular to said first major surface", and "a conductive path from said first power electrode to said second power electrode includes at least one vertical component in said semiconductor die", as recited in claims, 30, 41 and 50.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 30-32, 35-36, 38, 41-43, 46-47 and 49-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of "a conductive path from said first power electrode to said second power electrode includes at least one vertical component oriented substantially perpendicular to said first major surface", "a conductive path from said source electrode to said drain electrode includes at least one vertical component oriented substantially perpendicular to said first major surface", and "a conductive path from said first power electrode to said second power electrode includes at least one vertical component in said semiconductor die", as recited in claims 30, 41 and 50, are unclear as to how the respective electrodes can have a vertical component which is generally perpendicular to said first major surface, since both electrodes are formed on one first major surface.

The claimed limitation of "said diffusion region", as recited in claims 30 and 41, is unclear as to whether said diffusion region is the same element as the "at least one diffusion region of a second conductivity type" recited earlier, or a different element.

The claimed limitation of "said first and second solder balls", as recited in claims 31-32 and 42-43, are unclear as to whether said first and second solder balls are the same elements recited earlier, or different elements.

The claimed limitation of "a highly doped region of said first conductivity type, said highly doped region in contact with a first power electrode", as recited in claim 50, is unclear as to the structural relationship between the highly doped region of said first conductivity type, the first power electrode and the claimed device.

The claimed limitation of "a high conductivity region connecting said highly doped substrate with a second power electrode formed", as recited in claim 50, is unclear as to

which element is formed and is the structural relationship between the second power electrode and the claimed device.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30, 35, 38, 41, 46-47 and 49-50, 53, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Shoji et al. (JP 10-313010).

Regarding claim 50, Shoji et al. teach in figure 9 and related text a flip-chip semiconductor device comprising:

a semiconductor die including a highly doped substrate 11 of a first conductivity type,

a P/N junction receiving layer 12 of said first conductivity type formed over said highly doped substrate, and

at least one diffusion region p- (p- layer between layers 13 and 16) of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped region N+ of said first conductivity type, said highly doped region in contact with a first power electrode 8;

a high conductivity region 18 connecting said highly doped substrate with a second power electrode 9 formed;

wherein a conductive path from said first power electrode to said second power electrode includes at least one vertical component in said semiconductor die.

Regarding claims 30 and 41, Shoji et al. teach in figure 9 and related text a semiconductor device comprising:

a semiconductor die having a first major surface and a second major surface opposite from and substantially parallel to said first major surface, said semiconductor die including a highly doped substrate 11 of a first conductivity type,

a P/N junction receiving layer 12 of said first conductivity type formed over said highly doped substrate, and

at least one diffusion region p- (p- layer between layers 13 and 16) of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped region N+ of said first conductivity type formed in said diffusion region, said highly doped region in contact with a first power electrode 8 formed over said first major surface;

a high conductivity region 18 connecting said highly doped substrate with a second power electrode 9 formed over said first major surface and laterally spaced apart from said first power electrode;

wherein a conductive path from said first power electrode to said second power electrode includes at least one vertical component oriented substantially perpendicular to said first major surface.

Kitamura et al. do not explicitly state in the embodiment of figure 15 using the device in a flip chip arrangement.

Regarding claim 41, Shoji et al. teaches a highly doped source region of said first conductivity type formed in said diffusion region adjoining an insulated gate structure of said flip-chip semiconductor device, said highly doped source region in contact with a source electrode S formed over said first major surface, and a high conductivity region connecting (electrically connecting) said highly doped substrate with a drain electrode formed over said first major surface and laterally spaced apart from said source electrode.

Regarding claims 35, 38, 46-47, 49 and 53, Shoji et al. teach in figure 9 and related text said high conductivity region connecting said highly doped substrate with said second power electrode comprises a highly doped sinker region of said first conductivity type, and

a control electrode (gate) formed over said first major surface, and

a gate electrode formed over said first major surface and laterally spaced from said source electrode and said drain electrode, wherein

said insulated gate structure is situated entirely over said first major surface, wherein

said high conductivity region connecting said highly doped substrate with said drain electrode is one of a highly doped sinker region of said first conductivity type, and a metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface, and wherein said high conductivity region connecting said highly doped substrate with said second power electrode comprises a highly doped sinker region of said first conductivity type.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-32, 36, 42-43, 51-52 and 54, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji et al. in view of Rinne et al. (6,117,299).

Regarding claims 31-32, 42-43 and 51-52, Shoji et al. teach in figure 9 and related text substantially the entire claimed structure, as recited in the claims above, except a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, wherein said first and second solder balls have a width of greater than or equal to approximately 200 microns and wherein said first and second solder balls are separated by a pitch of greater than or equal to approximately 0.8 mm,

and a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode.

Rinne et al. teach in figure 3 and related text a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, and a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to connect a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, wherein said first and second solder balls have a width of greater than or equal to approximately 200 microns and wherein said first and second solder balls are separated by a pitch of greater than or equal to approximately 0.8 mm, and a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode, in Shoji et al.'s device, in order to operate the device in its intended use by providing economical external connections to the device, and in order to optimize the device characteristics by using specific solder balls width and pitch, respectively. It has been held that discovering an optimum value of a result effective variable of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPA 215 (CCPA 1980).

Regarding claims 36 and 54, prior art does not teach said high conductivity region connecting said highly doped substrate with said second power electrode comprises a

metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use said high conductivity region connecting said highly doped substrate with said second power electrode comprises a metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface, in prior art's device in order to have better control over the conductivity and the electrical characteristics of the high conductivity element.

Claims 30, 35, 38, 41, 46-47 and 49-50, 53, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al. (6,831,331).

Regarding claim 50, Kitamura et al. teach in figure 15 and related text a semiconductor device comprising:

a semiconductor die including a highly doped substrate 207 (at least part of the substrate) of a first conductivity type,

a P/N junction receiving layer 208 of said first conductivity type formed over said highly doped substrate, and

at least one diffusion region 209 of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped region 217 of said first conductivity type, said highly doped region in contact with a first power electrode D;

a high conductivity region 226a connecting said highly doped substrate with a second power electrode S formed;

wherein a conductive path from said first power electrode to said second power electrode includes at least one vertical component in said semiconductor die.

Kitamura et al. do not explicitly state in the embodiment of figure 15 using the device in a flip chip arrangement.

Kitamura et al. teach in column 11, lines 57-60 using the electrodes of the device as bump electrodes in a flip chip arrangement.

It would have been obvious to one having ordinary skill in the art at the time the invention was made use Nakagawa et al.'s device in a flip chip arrangement, in order to use the device in an application which requires flip chip arrangement.

Regarding claims 30 and 41, Kitamura et al. teach in figure 15 and related text a semiconductor device comprising:

a semiconductor die having a first major surface and a second major surface opposite from and substantially parallel to said first major surface, said semiconductor die including a highly doped substrate 207 (at least part of the substrate) of a first conductivity type,

a P/N junction receiving layer 208 of said first conductivity type formed over said highly doped substrate, and

at least one diffusion region 209 of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped region 217 of said first conductivity type formed in said diffusion region, said highly doped region in contact with a first power electrode D formed over said first major surface;

a high conductivity region 226a connecting said highly doped substrate with a second power electrode S formed over said first major surface and laterally spaced apart from said first power electrode (the vertical lines which touch the substrate);

wherein a conductive path from said first power electrode to said second power electrode includes at least one vertical component oriented substantially perpendicular to said first major surface.

Kitamura et al. do not explicitly state in the embodiment of figure 15 using the device in a flip chip arrangement.

Kitamura et al. teach in column 11, lines 57-60 using the electrodes of the device as bump electrodes in a flip chip arrangement.

It would have been obvious to one having ordinary skill in the art at the time the invention was made use Kitamura et al.'s device in a flip chip arrangement, in order to use the device in an application which requires flip chip arrangement.

Regarding claim 41, Kitamura et al. teach a highly doped source region 215 of said first conductivity type formed in said diffusion region adjoining an insulated gate structure of said flip-chip semiconductor device, said highly doped source region in contact with a source electrode S formed over said first major surface, and a high conductivity region connecting (electrically connecting) said highly doped substrate with a drain electrode

formed over said first major surface and laterally spaced apart from said source electrode.

Regarding claims 35, 38, 46-47, 49 and 53, Kitamura et al. teach in figure 15 and related text said high conductivity region connecting said highly doped substrate with said second power electrode comprises a highly doped sinker region of said first conductivity type, and

a control electrode formed over said first major surface, and

a gate electrode formed over said first major surface and laterally spaced from said source electrode and said drain electrode, wherein

said insulated gate structure is situated entirely over said first major surface, wherein said high conductivity region connecting said highly doped substrate with said drain electrode is one of a highly doped sinker region of said first conductivity type, and a metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface, and wherein

said high conductivity region connecting said highly doped substrate with said second power electrode comprises a highly doped sinker region of said first conductivity type.

Claims 31-32, 36, 42-43, 51-52 and 54, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al. (6,831,331) in view of Rinne et al. (6,117,299).

Regarding claims 31-32, 42-43 and 51-52, Kitamura et al. teach in figure 15 and related text substantially the entire claimed structure, as recited in the claims above, except a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, wherein said first and second solder balls have a width of greater than or equal to approximately 200 microns and wherein said first and second solder balls are separated by a pitch of greater than or equal to approximately 0.8 mm, and a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode.

Rinne et al. teach in figure 3 and related text a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, and a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to connect a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, wherein said first and second solder balls have a width of greater than or equal to approximately 200 microns and wherein said first and second solder balls are separated by a pitch of greater than or equal to approximately 0.8 mm, and a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode, in Kitamura et al.'s device, in order to operate the device in its intended use by providing economical external connections to the device, and in order to optimize the device characteristics by using specific solder balls width and pitch,

respectively. It has been held that discovering an optimum value of a result effective variable of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPA 215 (CCPA 1980).

Regarding claims 36 and 54, prior art does not teach said high conductivity region connecting said highly doped substrate with said second power electrode comprises a metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to use said high conductivity region connecting said highly doped substrate with said second power electrode comprises a metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface, in Kitamura et al.'s device in order to have better control over the conductivity and the electrical characteristics of the high conductivity element.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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